# **Kunpeng Wang**

I'm enthusiastic about formal verification, architecture design, and system security. I have strong self-learning and hands-on practical skills, and aim to pursue impactful and practical works.

#### **EDUCATION**

# **Shanghai Jiao Tong University**

Sep.2022 ~ Present

B.Eng. of Computer Science and Technology, Student in ACM Class

- Academic credit score: 90.4/100.
- Selected courses: Program Verification: 99, Programming Practice: 100, Compiler Design: 96, Operating System: 95, Algorithms: 98, Comprehensive Design for Computer System: 95.

#### RESEARCH

## **MATCHA Group**, MIT

May.2024 ~ Dec.2025

Advised by Prof. Mengjia Yan

Research Topic: secure (out-of-order) processor design and verification.

# **Uninterpreted Function for Contract Verification, ongoing**

- Use model checking to verify the contract property on out-of-order processor.
- Architectural insight guided proving and verification oriented hardware design.
- Plan to submit to S&P 2026

# Network Security and Privacy Protection (NSEC) Lab, SJTU

June.2024 ~ June.2026

Advised by *Prof. Guoxing Chen* 

Research Topic: verifiable interrupt-based side-channel mitigation for trusted execution environment.

## Verifiable Contract for TEE, ongoing

- Contract between mutual distrust TEE and OS to mitigate interrupt-based side-channel attacks.
- Allow both TEE and OS to verify the contract and generate proof of execution.

#### **COURSE PROJECTS**

## Verified TypeInfer, **©**

Spring 2024

- Use Coq to verify the correctness of a type inference algorithm implemented by C.
- 2k lines of Coq code.

Mx-Compiler, Summer 2023

- A compiler from Mx language (a variant of C++ language designed for course) to RISCV32IM assembly
- Features: Graphing Coloring, Mem2Reg, Constant Propagation, etc.
- 15.8k lines C++ code.

#### RISCV32I CPU, 🗘

Fall 2023

- Features: Tomasulo, Branch Prediction, Instruction Cache, etc.
- Could run on a Xilinx FPGA board.
- 3.3k lines of Verilog code.

#### RISCV64 Macrokernel,

Spring 2024

- Features: KASLR, Virtual Memory, Buddy Allocator, Unix-like Syscall, etc.
- Tested on real hardware, VisionFive2.
- Also implemented SBI (boot loader for RISC-V).
- 3k lines of Rust code.

## TEACHING ASSISTANT EXPERIENCE

<b>Programming (C++)</b> , Huiyu Weng	Fall 2023	Data Structure, Alei Liang	Summer 2024
Data Structure, Huiyu Weng	Spring 2024	<b>Programming Practice</b> , Yong Yu	Summer 2024

Last updated: 2025-09-29 Kunpeng Wang